ZY2105 5A No-Bus POL Data Sheet
8V to 14V Input • 0.5V to 5.5V Output

power-one® Changing the Shape of Power

Member of the maXyz Family

RoHS Compliant

Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessor applications
- Industrial computing, servers, and storage
- Broadband, networking, optical, and wireless communications systems
- Active memory bus terminators

Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components and communication bus
- Completely programmable via pin strapping and one external resistor
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 8V–14V
- High continuous output current: 5A
- Wide programmable output voltage range: 0.5V–5.5V
- Output voltage margining
- Overcurrent and overtemperature protections
- Overvoltage and undervoltage protections, and Power Good signal tracking the output voltage setpoint
- Tracking during turn-on and turn-off with guaranteed slew rates
- Sequenced and cascaded modes of operation
- Single-wire line for frequency synchronization between multiple POLs
- Programmable feedback loop compensation
- Enable control
- Flexible fault management and propagation
- Start-up into the load pre-biased up to 100%
- Current sink capability
- Industry standard size through-hole single-in-line package: 1.2”x0.26”
- Low height of 0.84”
- Wide operating temperature range: 0 to 70ºC
- UL 60950-1/CSA 22.2 No. 60950-1-07 Second Edition, IEC 60950-1: 2005, and EN 60950-1:2006

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Description

Power-One’s point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZY2105 is an intelligent, fully programmable step-down point-of-load DC-DC module integrating digital power conversion and power management. The ZY2105 completely eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. Performance parameters of the ZY2105 are programmable by pin strapping and an external resistor and can be changed by the user at any time during product development and service without a need for a communication bus.

Reference Documents

No-Bus™ POL Converters. Application Note
Z-One® POL Converters. Eutectic Solder Process Application Note
Z-One® POL Converters. Lead-Free Process Application Note

1. Ordering Information

ZY	21	05	y	–	zz
Product family: Z-One Module	**Series:** No-Bus POL Converter	**Output Current:** 5A	**RoHS compliance:** **No suffix** - RoHS compliant with Pb solder exemption[1] **G** - RoHS compliant for all six substances	**Dash**	**Packaging Option[2]:** **R1** – 48 pcs Tray **Q1** – 1 pc sample for evaluation only

[1] The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.
[2] Packaging option is used only for ordering and not included in the part number printed on the POL converter label.

Example: **ZY2105G-R3**: A 48-piece tray of RoHS compliant POL converters. Each POL converter is labeled ZY2105G.

2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the POL converter.

Parameter	Conditions/Description	Min	Max	Units
Operating Temperature	Controller Case Temperature	-40	105	°C
Input Voltage	250ms Transient		15	VDC

3. Environmental and Mechanical Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Ambient Temperature Range		0		70	°C
Storage Temperature (Ts)		-55		125	°C
Weight				6	grams
Operating Vibration (sinusoidal)	Frequency Range Magnitude Sweep Rate Repetitions in each axis (Min-Max-Min Sweep)	5 0.5 1 2		500	Hz G oct/min sweeps
Non-Operating Shock (half sine)	Acceleration Duration Number of shocks in each axis	50 11 10			G ms
MTBF	Calculated Per Telcordia Technologies SR-332	TBD			MHrs
Peak Reflow Temperature	ZY2105			220	°C
Peak Reflow Temperature	ZY2105G		245	260	°C
Lead Plating	ZY2105 and ZY2105G	100% Matte Tin			
Moisture Sensitivity Level	JEDEC J-STD-020C	3			

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4. Electrical Specifications

Specifications apply at the input voltage from 8V to 14V, output load from 0 to 5A, ambient temperature from 0°C to 70°C, output capacitance consisting of 3x22µF ceramics and a 47µF tantalum, and the CCA=0 unless otherwise noted.

4.1 Input Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Input voltage (V_{IN})		8		14	VDC
Undervoltage Lockout Threshold	Ramping Up Ramping Down		7.2 6.8		VDC VDC
Input Current	V_{IN}=12V, POL is OFF		19		mADC
Maximum Input Current	V_{IN}=8V, V_{OUT}=5.5V			3.7	ADC

4.2 Output Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Output Current (I_{OUT})	$V_{IN\ MIN}$ to $V_{IN\ MAX}$	-5[1]		5	ADC
Output Voltage Range (V_{OUT})	Programmable with a resistor between TRIM and MARGIN pins Default (no resistor)	0.5	 0.5	5.5	VDC VDC
Output Voltage Setpoint Accuracy[2]	V_{IN}=12V, I_{OUT}=0.5*$I_{OUT\ MAX}$, room temperature	±1.5% or 20mV whichever is greater			$\%V_{OUT}$
Line Regulation[2]	$V_{IN\ MIN}$ to $V_{IN\ MAX}$		±0.5		$\%V_{OUT}$
Load Regulation[2]	0 to $I_{OUT\ MAX}$		±0.5		$\%V_{OUT}$
Dynamic Regulation Peak Deviation Settling Time	50% – 100% – 50% load step, Slew rate 2.5A/µs, to 10% of peak deviation		 100 60		 mV µs
Output Voltage Peak-to-Peak Ripple and Noise BW=20MHz Full Load	V_{IN}=12V, V_{OUT}≤1.0V V_{IN}=12V, V_{OUT}=2.5V V_{IN}=12V, V_{OUT}=5.0V		 15 20 25		 mV mV mV
Efficiency V_{IN}=12V Full Load Room temperature	V_{OUT}=0.5V V_{OUT}=0.75V V_{OUT}=1.0V V_{OUT}=1.2V V_{OUT}=1.8V V_{OUT}=2.5V V_{OUT}=3.3V V_{OUT}=5.0V		63.2 71.5 76.8 79.8 84.8 87.9 90.0 92.4		% % % % % % % %
Temperature Coefficient	V_{IN}=12V, I_{OUT}=0.5*$I_{OUT\ MAX}$, V_{OUT}=5V		60		ppm/°C
Switching Frequency		450	500	550	kHz

[1] At the negative output current (bus terminator mode) efficiency of the ZY2105 degrades resulting in increased internal power dissipation. Therefore maximum allowable negative current under specific conditions is 20% lower than the current determined from the derating curves shown in paragraph 5.5

[2] Digital PWM has an inherent quantization uncertainty of ±6.25mV that is not included in the specified static regulation parameters.

4.3 Protection Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Output Overcurrent Protection					
Type		Non-Latching, 130ms period			
Threshold			155		$\%I_{OUT}$
Threshold Accuracy		-25		25	$\%I_{OCP.SET}$
Output Overvoltage Protection					
Type		Latching			
Threshold	Follows the output voltage setpoint		130[1]		$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{OVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Output Undervoltage Protection					
Type		Non-Latching, 130ms period			
Threshold	Follows the output voltage setpoint		75		$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{UVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Overtemperature Protection					
Type		Non-Latching, 130ms period			
Turn Off Threshold	Temperature is increasing		120		°C
Turn On Threshold	Temperature is decreasing after module was shut down by OTP		110		°C
Threshold Accuracy		-5		5	°C
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Power Good Signal (PGOOD pin)					
Logic	V_{OUT} is inside the PG window and stable V_{OUT} is outside of the PG window or ramping up/down	High Low			N/A
Lower Threshold	Follows the output voltage setpoint		90		$\%V_{O.SET}$
Upper Threshold	Follows the output voltage setpoint		110		$\%V_{O.SET}$
Delay	From instant when threshold is exceeded until status of PG pin changes		6		µs
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{O.SET}$

[1] Minimum OVP threshold is 1.0V

4.4 Feature Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Tracking					
Rising Slew Rate	Proportional to SYNC frequency		0.1		V/ms
Falling Slew Rate	Proportional to SYNC frequency		-0.5		V/ms
Enable (EN pin)					
EN Pin Polarity		Positive (enables the output when EN pin is open or pulled high)			
EN High Threshold		2.3			VDC
EN Low Threshold				1.0	VDC
Open Circuit Voltage			3.3		VDC
Turn-On Delay	From EN pin changing state to V_{OUT} starting to ramp up		0		ms
Turn-Off Delay	From EN pin changing state to V_{OUT} reaching 0V		11		ms
Feedback Loop Compensation (CCA pin)					
CCA pin is open	Recommended C_{OUT}/ESR range, combination of ceramic + tantalum	50/5 + 220/40	100/5 + 470/40	400/5 + 2000/20	µF/mΩ µF/mΩ
CCA pin is connected to GND	Recommended C_{OUT}/ESR range, ceramic	100/5	220/5	400/5	µF/mΩ

NOT FOR NE

4.5 Signal Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
VDD	Internal supply voltage	3.15	3.3	3.45	V
SYNC Line					
ViL_s	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_s	HIGH level input voltage	0.75 x VDD		VDD + 0.5	V
Vhyst_s	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
IoL_s	LOW level sink current V(SYNC)=0.5V	14		60	mA
Ipu_s	Pull-up current source V(SYNC)=0V	300		1000	µA
Tr_s	Maximum allowed rise time 10/90%VDD			300	ns
Cnode_s	Added node capacitance		5	10	pF
Freq_s	Clock frequency of external SYNC line	475		525	kHz
Tsynq	Sync pulse duration	22		28	% of clock cycle
T0	Data=0 pulse duration	72		78	% of clock cycle
Inputs: CCA, EN, IM					
Iup_x	Pull-up current source V(X)=0	25		110	µA
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
RdnL_x	External pull down resistance pin forced low			10	kΩ
Power Good and OK Inputs/Outputs					
Iup_PG	Pull-up current source V(PG)=0	25		110	µA
Iup_OK	Pull-up current source V(OK)=0	175		725	µA
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
IoL_x	LOW level sink current at 0.5V	4		20	mA

NC

5. Typical Performance Characteristics

5.1 Efficiency Curves

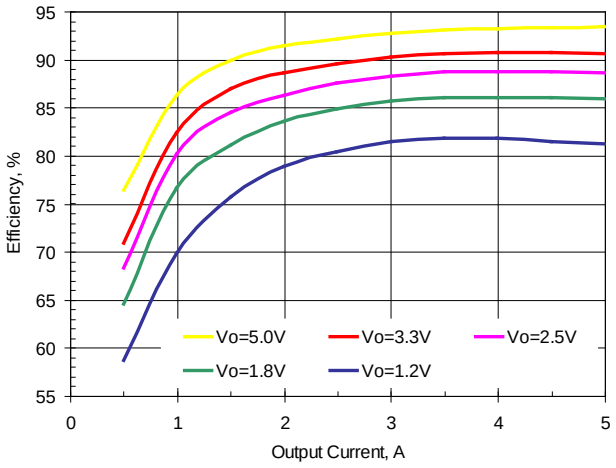

Figure 1. Efficiency vs. Load. Vin=9.6V

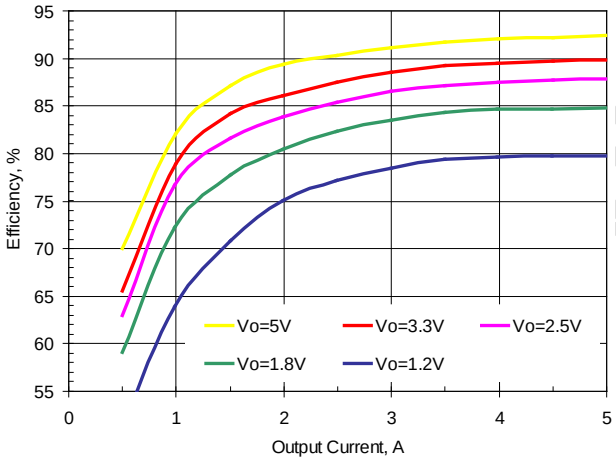

Figure 2. Efficiency vs. Load. Vin=12V

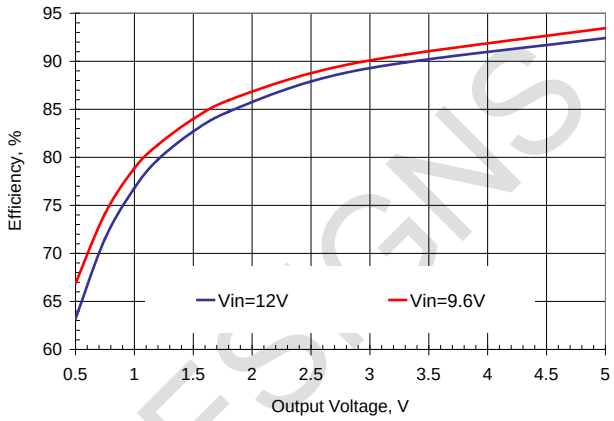

Figure 3. Efficiency vs. Output Voltage, Iout=5A

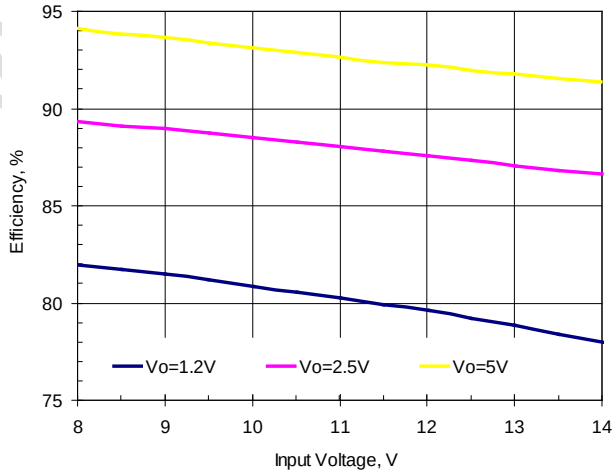

Figure 4. Efficiency vs. Input Voltage. Iout=5A

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5.2 Turn-On Characteristics

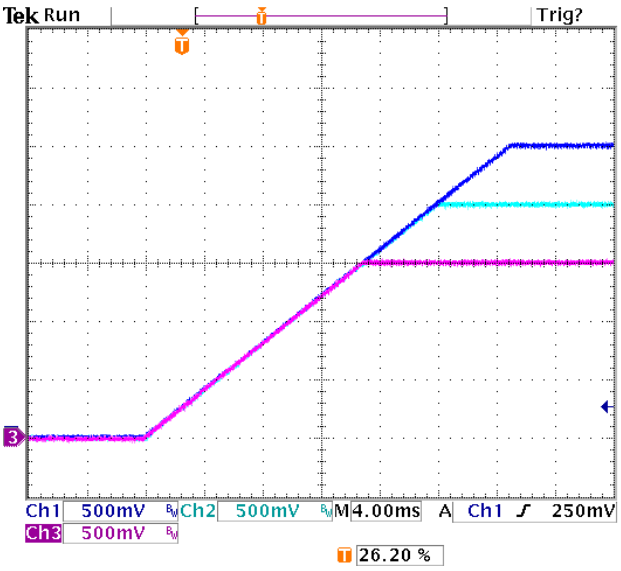

Figure 5. Tracking Turn-On.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

5.3 Turn-Off Characteristics

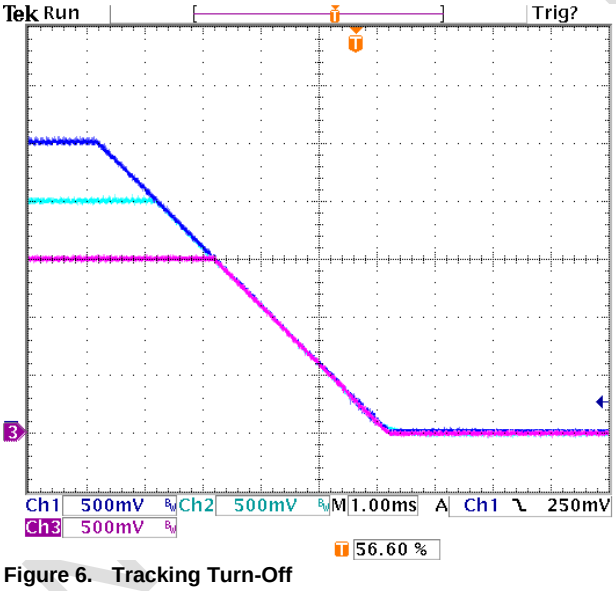

Figure 6. Tracking Turn-Off
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50%-100%-50% step load at 2.5A/µs. In all tests the POL converter had a total of 110µF ceramic and tantalum capacitors connected across the output pins. The speed of the transient response was varied by selecting different CCA settings.

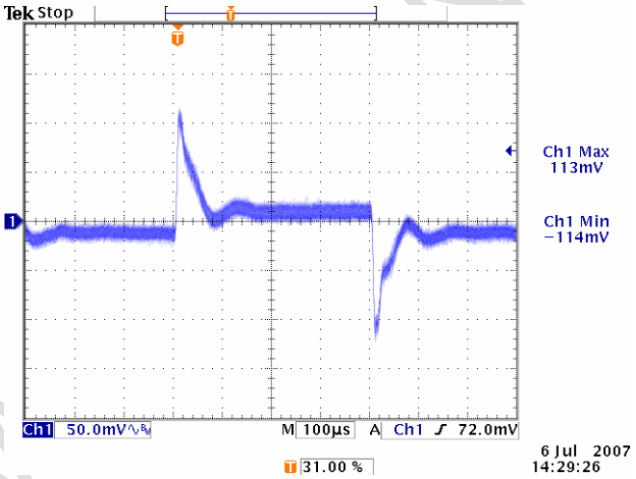

Figure 7. Vin=12V, Vout=5V. CCA=0

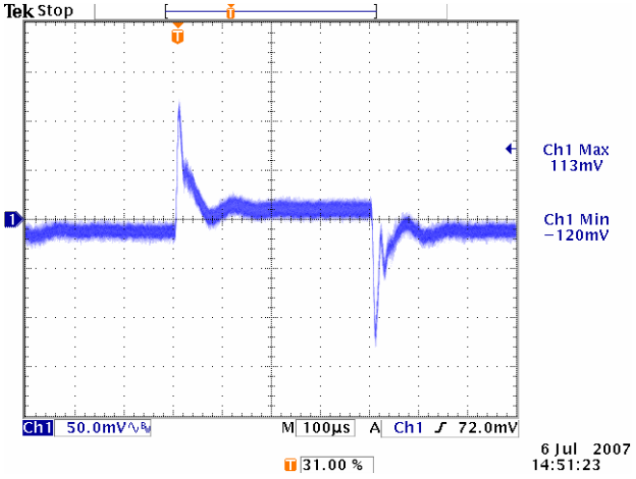

Figure 8. Vin=12V, Vout=5V. CCA=1

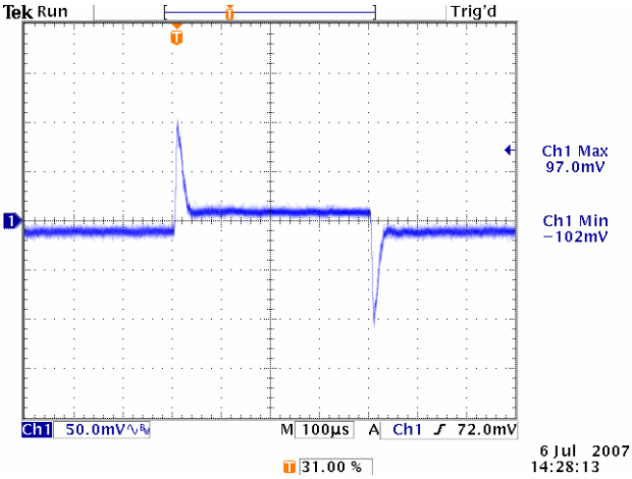

Figure 9. Vin=12V, Vout=1V. CCA=0

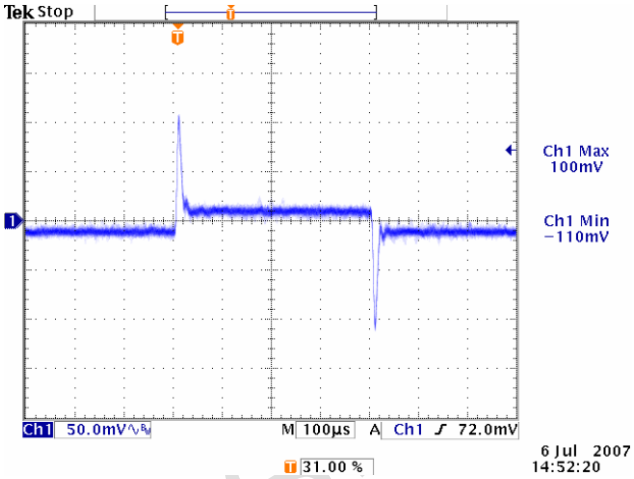

Figure 10. Vin=12V, Vout=1V. CCA=1

5.5 Thermal Derating Curve

Figure 11. Thermal Derating Curves. Vin=12V, Vout=5V

6. Typical Application

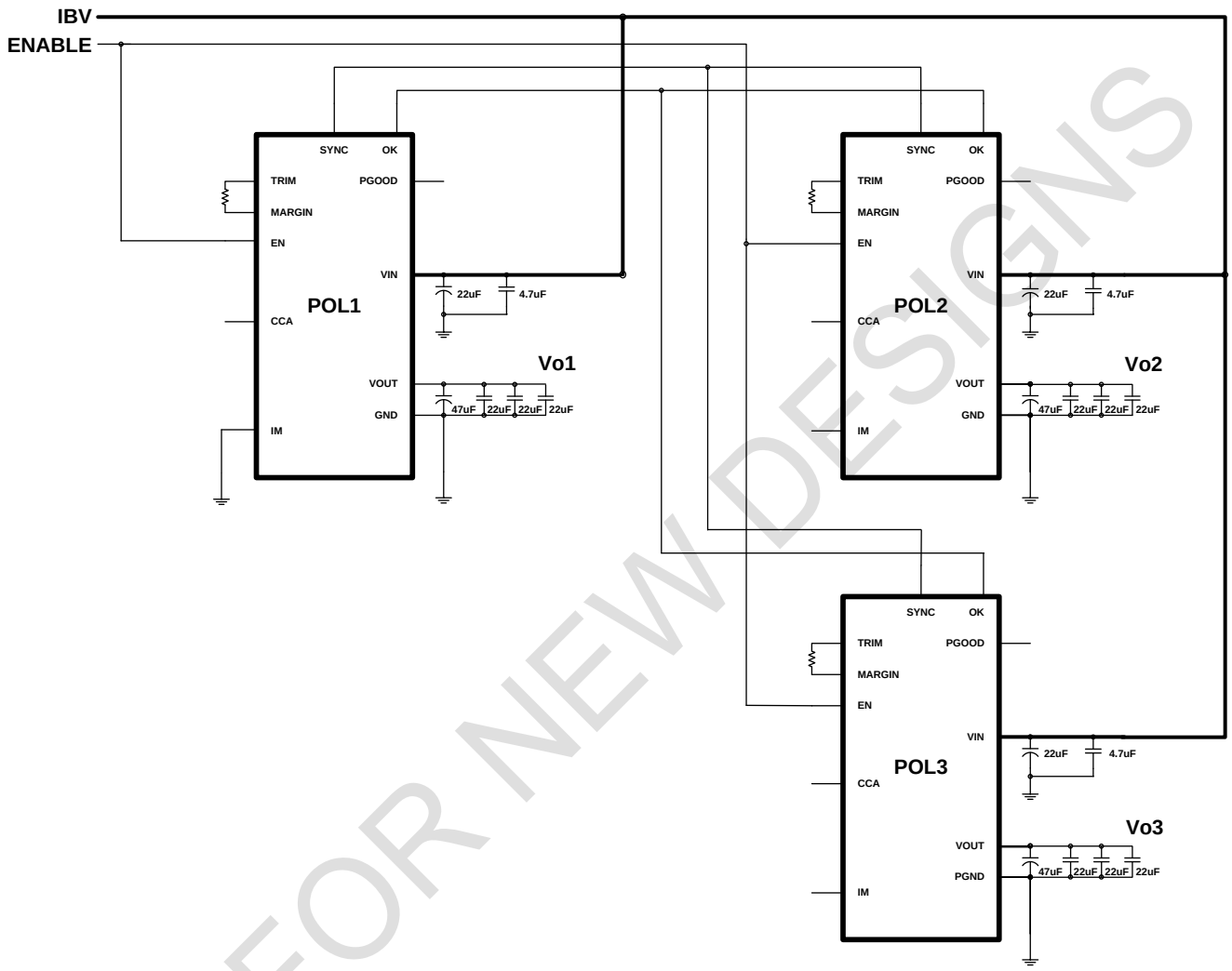

Figure 12. Complete Schematic of Application with Three Independent Outputs. Intermediate Bus Voltage is from 8V to 14V.

In this application three POL converters are configured to deliver three independent output voltages. Output voltages are programmed with the resistors connected between TRIM and MARGIN pins of individual converters.

POL1 is configured as a master (IM pin is grounded) and all other POL converters are synchronized to the switching frequency of POL1.

All converters are controlled by the common ENABLE signal. Turn-on and turn-off processes of the system are illustrated by pictures in Figure 5 and Figure 6.

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7. Pin Assignments and Description

Pin Name	Pin Number	Pin Type	Buffer Type	Pin Description	Notes
OK	8	I/O	PU	Fault Status	Connect to OK pin of other Z- POLs. Leave open, if not used
SYNC	9	I/O	PU	Frequency Synchronization Line	Connect to SYNC pin of other Z-POLs or to an external clock generator
PGOOD	6	I/O	PU	Power Good	
IM	10	I	PU	Master Mode	Tie to GND to make the POL the clock master or leave open to synchronize to external clock
CCA	2	I	PU	Compensation Coefficient Address	Tie to PGND for 0 or leave open for 1
MARGIN	3	A		Output Voltage Margining	To program the output voltage, connect a resistor between MARGIN and TRIM
EN	5	I	PU	Enable	POL is ON when the pin is high or floating. POL is OFF when the pin is low or connected to GND
TRIM	4	A		Output Voltage Trim	To program the output voltage, connect a resistor between MARGIN and TRIM
VOUT	1	P		Output Voltage	
GND	7	P		Power Ground	
VIN	11	P		Input Voltage	

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

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8. Pin and Feature Description

8.1 OK, Fault Status

The open drain input/output with the internal pull-up resistor. The POL converter pulls its OK pin low, if a fault occurs. Pulling low the OK input by an external circuitry turns off the POL converter.

8.2 SYNC, Frequency Synchronization Line

The bidirectional input/output with the internal pull-up resistor. If the POL converter is configured as a master, the SYNC line propagates clock to other POL converters. If the POL converter is configured as a slave, the internal clock recovery circuit synchronizes to the clock of the SYNC line.

8.3 IM, Interleave Mode

The input with the internal pull-up resistor. Pulling the IM pin low configures a POL converter as a master.

8.4 PG, Power Good

The open drain input/output with the internal pull-up resistor. The pin is pulled low by the POL converter, if the output voltage is outside of the window defined by the Power Good High and Low thresholds.

Note: See the No-Bus Application Note for recommendations on PG deglitching.

8.5 CCA, Compensation Coefficient Address

The input with internal pull-up to select one of 2 sets of digital filter coefficients optimized for different characteristics of output capacitance.

8.6 MARGIN, Output Voltage Margining

The output of the 2V internal voltage reference that is used to program the output voltage of the POL converter.

8.7 EN, Enable

The input with the internal pull-up resistor. The POL converter is turned off, when the pin is pulled low

8.8 TRIM, Output Voltage Trim

The input of the TRIM comparator for the output voltage programming.

The output voltage can be programmed by a single resistor connected between MARGIN and TRIM pins.

9. Application Information

9.1 Output Voltage Programming

Resistance of the trim resistor is determined from the equation below:

$$R_{TRIM} = \frac{20 \times (5.5 - V_{OUT})}{V_{OUT}}, \text{ kΩ}$$

where V_{OUT} is the desired output voltage in Volts.

If the R_{TRIM} is open or the TRIM pin is shorted to PGND, the V_{OUT}=0.5V.

9.2 Output Voltage Margining

Margining can be implemented by changing the resistance between the REF and TRIM pins.

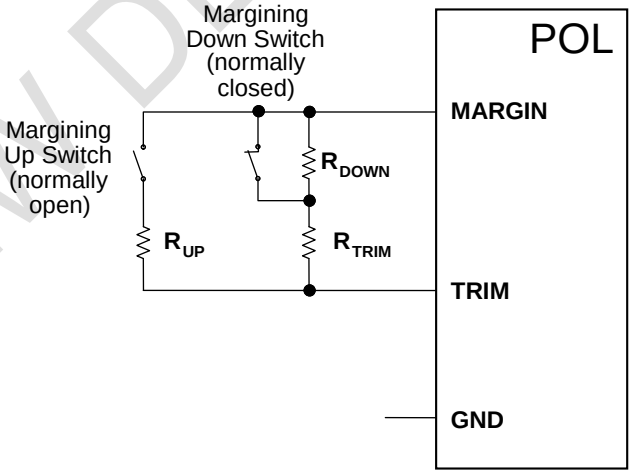

Figure 13. Margining Configuration

In the schematic shown in Figure 13, the nominal output voltage is set with the trim resistor R_{TRIM} calculated from the equation in the paragraph 9.1. Resistors R_{UP} and R_{DOWN} are added to margin the output voltage up and down respectively and determined from the equations below.

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

$$R_{DOWN} = (20 + R_{TRIM}) \times \left(\frac{\Delta V\%}{100 - \Delta V\%} \right), \text{ kΩ}$$

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where R_{TRIM} is the value of the trim resistor in kΩ and ΔV% is the absolute value of desired margining expressed in percents of the nominal output voltage.

During normal operation the resistors are removed from the circuit by the switches. The "Margining Down" switch is normally closed shorting the resistor R_{DOWN} while the "Margining Up" switch is normally open disconnecting the resistor R_{UP}.

An alternative configuration of the margining circuit is shown in Figure 14. In the configuration both switches are normally open that may be advantageous in some implementations.

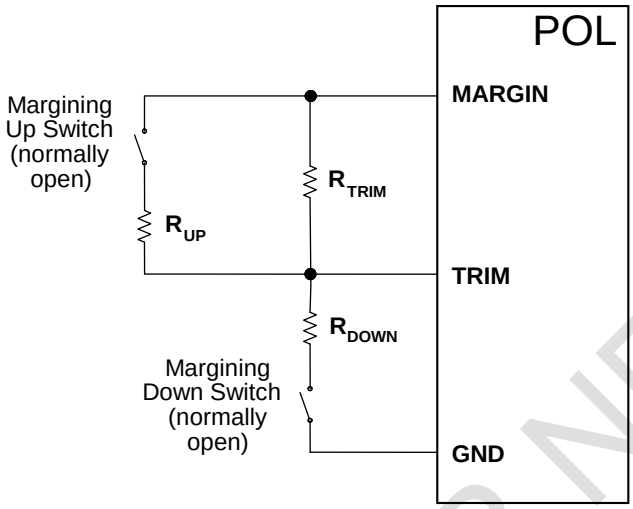

Figure 14. Alternative Margining Configuration

R_{UP} and R_{DOWN} for this configuration are determined from the following equations:

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

$$R_{DOWN} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{100 - \Delta V\%}{\Delta V\%} \right), \text{ kΩ}$$

Caution: Noise injected into the TRIM node may affect accuracy of the output voltage and stability of the POL converter. Always minimize the PCB trace length from the TRIM pin to external components to avoid noise pickup.

Refer to *No-Bus™ POL Converters. Application Note* on www.power-one.com for more application information on this and other product features.

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10. Mechanical Drawings

All Dimensions are in mm

Tolerances: XX.X: ±0.1 XX.XX: ±0.05

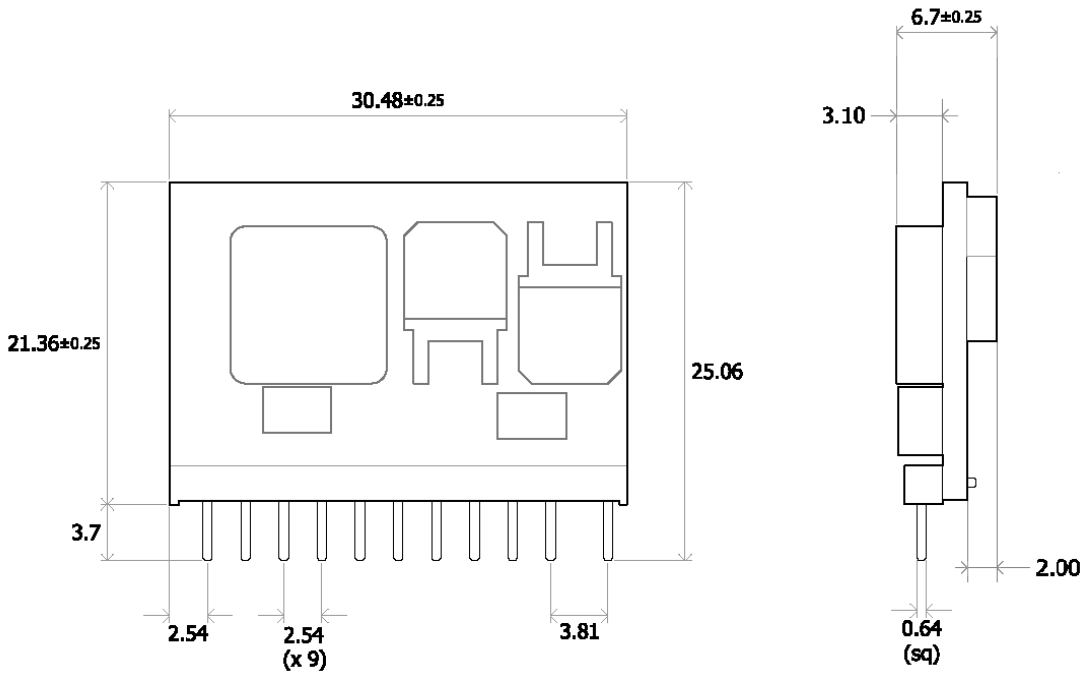

Figure 15. Mechanical Drawing

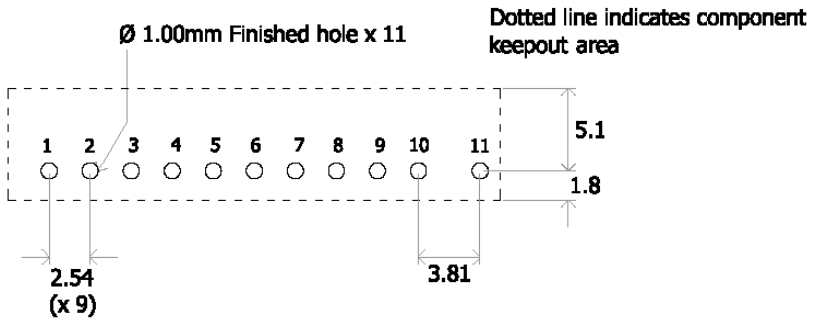

Figure 16. Recommended Footprint – Top View

Notes:

1. NUCLEAR AND MEDICAL APPLICATIONS - Power-One products are not designed, intended for use in, or authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the express written consent of the respective divisional president of Power-One, Inc.
2. TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

NOT RECOMMENDED